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US Army Research Laboratory

Same-Side Platinum Electrodes for Metal Assisted Etching of Porous Silicon

by Matthew H Ervin and Brian Isaacson

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14. ABSTRACT
We have developed new procedures for etching porous silicon (PSi), which will allow PSi devices to be more easily integrated with other devices used for initiating, controlling, or utilizing the output of the PSi devices. Of the 2 processes developed, the sacrificial electrode process is the simplest, but it produces an inhomogeneous PSi thickness across the wafer and introduces surface topography due to electro-polishing. By using the anchored electrode method, which incorporates a dielectric layer, more controllable etch depths and patterned devices are obtainable. One complication is that a proximity effect is observed where features closer to the electrode etch more rapidly. A simple voltage divider model can be used to predict the relative etch rates, but more work is required before a quantitative model for predicting etch depth will be possible. In order to vary the etch depth by varying the local electrode/silicon (Si) ratio, the electrode will need to be cut up into electrically isolated sections or else the carriers will conduct along the length of the electrode causing more etching at the most easily reached exposed Si.

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1. Introduction

A process for etching porous silicon (PSi) on the same side as the platinum (Pt) electrodes used to catalyze the etch has been developed. This is important as it provides significantly more flexibility for integrating PSi with other devices on the same wafer or chip. Currently, PSi is being used in a wide range of applications including optoelectronic devices, sensors, drug delivery, and on-chip energetics, to name a few. However, PSi is produced electrochemically using an aggressive etch solution containing a large fraction of concentrated hydrofluoric acid (HF) with which many materials and devices are not compatible. Being able to limit the PSi processing to one side of the wafer will facilitate the integration of PSi onto chips with other devices and functionalities.

PSi is most commonly formed by anodic etching of a silicon (Si) wafer in an etch solution containing a high concentration of HF (Korotcenkov and Cho 2010). Controlling this reaction requires some complexity as an electrical connection to the wafer must be made and a potentiostat is used to control the electrochemical etch current. In addition, an ultraviolet (UV) light source is required when etching n-type wafers. We have focused on using a metal-assisted etch, also referred to as a galvanic etch, which is a simplified etch procedure that does not require a potentiostat or external wires to the wafer. In this approach, a metal (e.g., silver [Ag], Pt, palladium [Pd], copper [Cu], and gold [Au]) is deposited on 1 side of a Si wafer, and this metallized wafer is immersed in a HF, hydrogen peroxide (H_2O_2), and ethanol etch solution. The H_2O_2 reacts with hydrogen ions from the HF at the catalytic metal surface to become water molecules while liberating electron-hole (h+) charge carriers into the metal/wafer. These h+ charge carriers traverse the wafer to the other side where they induce the exposed Si to react with the HF to produce a soluble dihydrogen silicon hexafluoride product (Le and Bohn 2000). In this arrangement, the HF and H_2O_2 concentrations control the electrochemical current, and therefore reaction rate, without any external instrumentation. In addition, the Pt to Si surface area ratio also affects the etch rate, as the etch current is proportional to the area of exposed Pt, and the area of exposed Si determines the resultant etch current density. If the current density at the Si surface becomes too large, the etch transitions from producing PSi to an electropolishing regime where the Si is completely etched away (Korotcenkov and Cho 2010).

2. Methodology

Two approaches were taken for using same-side Pt electrodes. In the first approach, Pt electrodes were deposited directly on the Si wafer to be etched. This approach is

termed the sacrificial Pt electrode approach since it is expected that the PSi etch will etch the Si underneath the Pt, eventually releasing the Pt from the wafer. In the second approach, termed the anchored Pt electrode approach, the Pt electrodes are deposited onto a Si wafer that is covered with a patterned silicon nitride (Si_3N_4) layer. This dielectric Si_3N_4 layer has openings in it to expose the Si to the PSi etch, and make electrical contact with the Pt electrodes deposited on top of the Si_3N_4.

In this study process, 1–10 Ω p+ Si wafers were used as they produce nanoporous Si, which is desired for our energetic PSi applications. These wafers have 500 nm of Si_3N_4 on both sides as received from Rogue Valley Microdevices. In the case of the sacrificial Pt electrodes, the nitride is entirely removed from 1 side of the wafer while, in the case of anchored Pt electrodes, photolithographically defined windows are etched in the nitride to expose Si areas for etching and for electrical contact to the Pt. These nitride etches are carried out using a Unaxis VLR 700 reactive ion etch system.

Once the nitride has been removed as desired, the Pt is sputter deposited onto the wafer. First the wafer is etched for 2 min in 6:1 H_2O:HF to remove any oxide that may have formed since the nitride etch. Then the wafer is sputter cleaned for 30 s in the Unaxis Clusterline 200 sputter deposition system. Without breaking vacuum, the samples are then transferred to the Pt sputter chamber where 170 nm of Pt is sputter deposited at a sample temperature of 250 °C. Next this Pt layer is patterned using photolithography and a 4Wave Inc 4W-PSIBE ion beam etch system.

The resulting wafers that have patterned Pt electrodes and exposed Si are then etched with a HF, ethanol, and peroxide mixture. The ethanol reduces the viscosity/surface tension of the etch solution so that it can penetrate into the small pores being formed. A typical etch composition is 3:1 HF:ethanol with 2.4% peroxide added; however, many variations in concentrations and etch times were used in this work.

The etch results were characterized using scanning electron microscope (SEM) cross-sectional micrographs obtained with a Hitachi S4500 SEM. Etch depth measurements were also made, after removing the PSi with a 1M potassium hydroxide (KOH) etch, using a Wyko NT1100 optical profilometer. In order to measure the combustion rates of the PSi, bridge wires were photolithographically deposited onto the wafers, prior to PSi etching, using a lift-off approach with metal deposited using a CHA Industries e-beam evaporator. In order to burn the PSi an oxidizer is applied to the PSi in the form of a 3 M sodium perchlorate in methanol solution. After drying for 30 min, the PSi is ignited by passing 20 V/1 A of current across the bridge wire. This is done while synchronously triggering a Photron

Devices Inc, high-speed camera, which is used to record the PSi burn in order to measure the burn rate.

3. Results and Discussion

3.1 Sacrificial Pt Electrodes

The sacrificial Pt approach was investigated because it is the simplest approach to same-side Pt electrodes as it requires only a Pt deposition and patterning process before the PSi etch. Figure 1 is a drawing showing the sample structure and associated etch process.

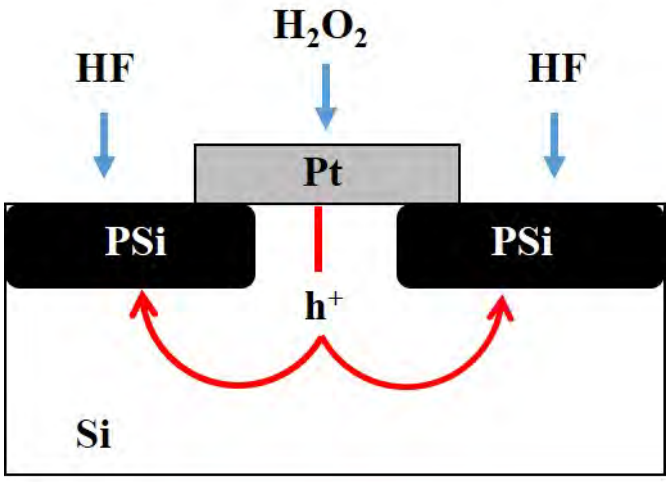

Fig. 1 Cross-sectional drawing of the sacrificial electrode structure and etch process depicting the PSi etch undercutting the Pt electrode

With a typical backside Pt electrode and a patterned opening in the topside Si_3N_4 to define the PSi etch area, the lateral PSi etching underneath the Si_3N_4 is approximately equal to the PSi etch depth as is shown in Fig. 2.

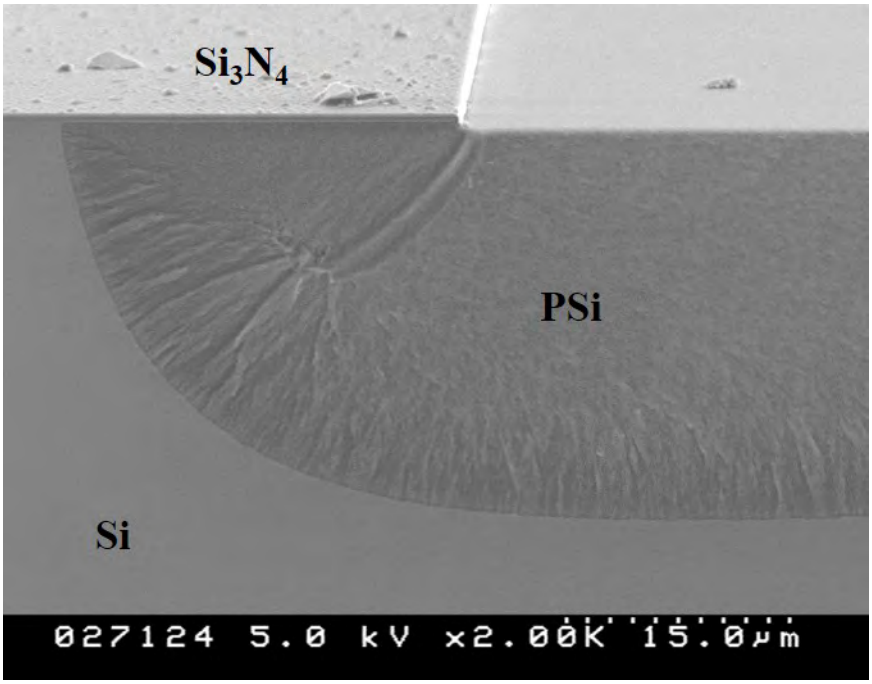

Fig. 2 SEM cross-sectional image showing PSi etching underneath the Si_3N_4 defining the Si exposed to the PSi etch

Given the expected isotropic PSi etching that undercuts the edges of the Si_3N_4 windows, topside sacrificial Pt electrodes were designed to be at least as wide as the desired etch depth. In this way, it was expected that the Pt would not be completely undercut until the desired etch depth had been achieved. In addition, by varying the width ratio of the Pt electrodes and the exposed Si, the etch current density and therefore etch rate should be controllable. Unfortunately, this turns out to be an overly simplified model of the etch process. In practice, the PSi etching under the Pt edges can enable the Pt to detach and peel back from the Si surface. As a result, the Pt can retreat from the etch-front producing greater lateral etching than the vertical etch depth as shown in Fig. 3.

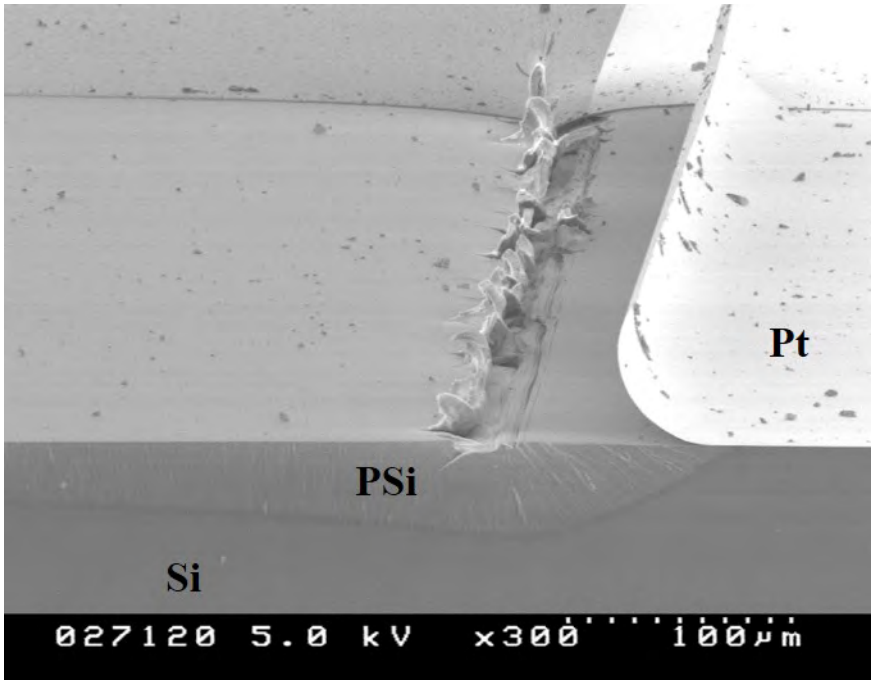

Fig. 3 SEM cross-sectional image showing a Pt electrode peeling back from the PSi etch-front resulting in greater lateral etching under the Pt than the vertical etching into the Si surface

This enhanced lateral etching under the Pt can be made even worse due to current crowding at the edges of the Pt electrodes (Murrmann and Widmann 1969). The current crowding is due to the Pt electrode being more conductive than the Si wafer so that the path of least resistance for the carriers is to conduct through the Pt and to transfer to the Si wafer surface primarily near the edge of the Pt in contact with the Si. There is then an enhanced etch rate near this Pt edge, since there is an additional resistance associated with conducting through the Si to etch sites farther from the Pt. This current crowding can increase the etch current density at the electrode edges into the electropolishing regime. An example of this is seen in the SEM cross-sectional image shown in Fig. 4, where the edges of the Pt electrodes can be seen to be undercut by about 8 microns while the PSi etch depth in the exposed Si area is less than 1 micron.

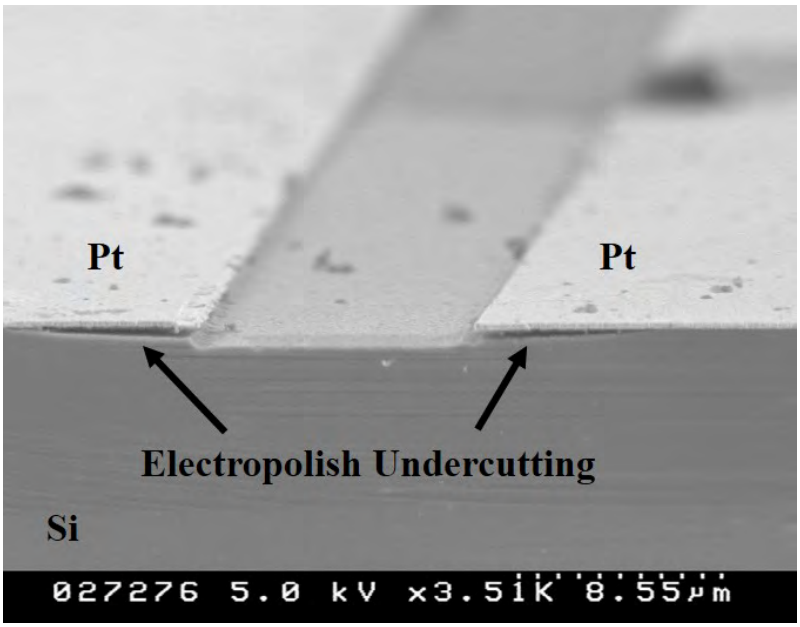

Fig. 4 SEM cross-sectional image showing undercutting of the Pt electrodes by electropolishing that is significantly more than the etch depth of the PSi in the exposed Si

In many cases, the etch results in the Pt being released from the Si surface leaving behind a curved surface in the area that was underneath the Pt, as shown in Fig. 5. It appears that the electropolishing is greatest at the beginning of the etch. As more Pt is undercut, there is more Si exposed so that the Pt:Si ratio drops. This, in turn, reduces the etch current density and therefore reduces the electropolishing of the underlying Si.

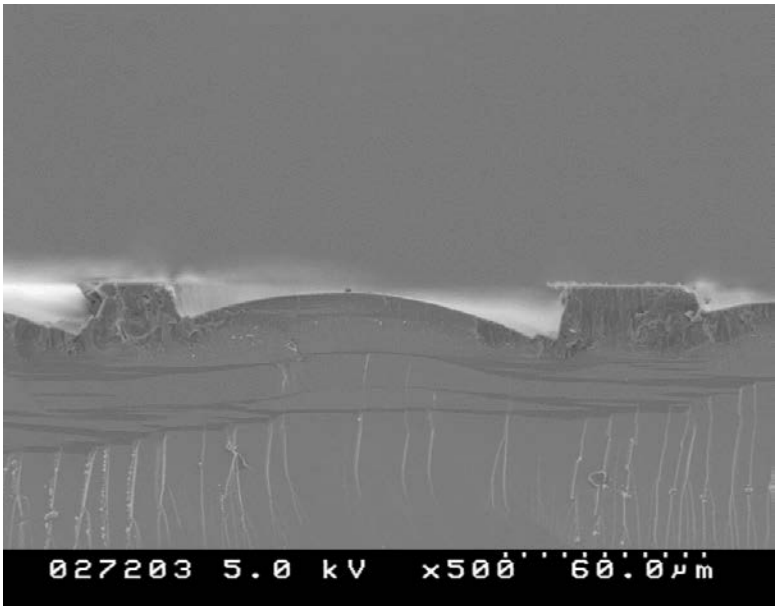

Fig. 5 SEM cross-sectional image showing that undercutting of the Pt electrodes by electropolishing can leave a curved surface on the underlying Si/PSi

In order to minimize the deleterious electropolishing, the etch solution was changed to minimize the etch current by reducing the H_2O_2 concentration or the H_2O_2 and HF concentrations. One approach was to put the sample into 20 ml of ethanol and then adding 1 ml of the normal etch solution every minute for 30 min and then continuing the etch at that final 60% of normal concentration for another 30 min. Figure 6 shows the results of such an etch. The thickest PSi (9 microns) occurs in a narrow Si window with gradually thinning PSi underneath where the Pt was. This is the thickest PSi produced to this point with sacrificial Pt electrodes. While more experimenting with the etch solution and Pt:Si ratio may enable thicker PSi, it still appears that the PSi thickness will be non-uniform across the sample surface. This is likely to adversely affect the energetic performance of the inhomogeneous PSi film for many applications. Even if the Pt electrodes could be induced to stay adhered to the Si surface throughout the etch, it is possible that once PSi has etched completely underneath it, that the etch would then stop or greatly slow. This is because the PSi should be significantly more resistive than the unetched Si. It is believed that the reason the pore side walls do not etch is because they are fully depleted of carriers (Korotcenkov and Cho 2010). In order to achieve thicker PSi films along with better control over the PSi pattern on the wafer, the anchored Pt approach was developed as is discussed next.

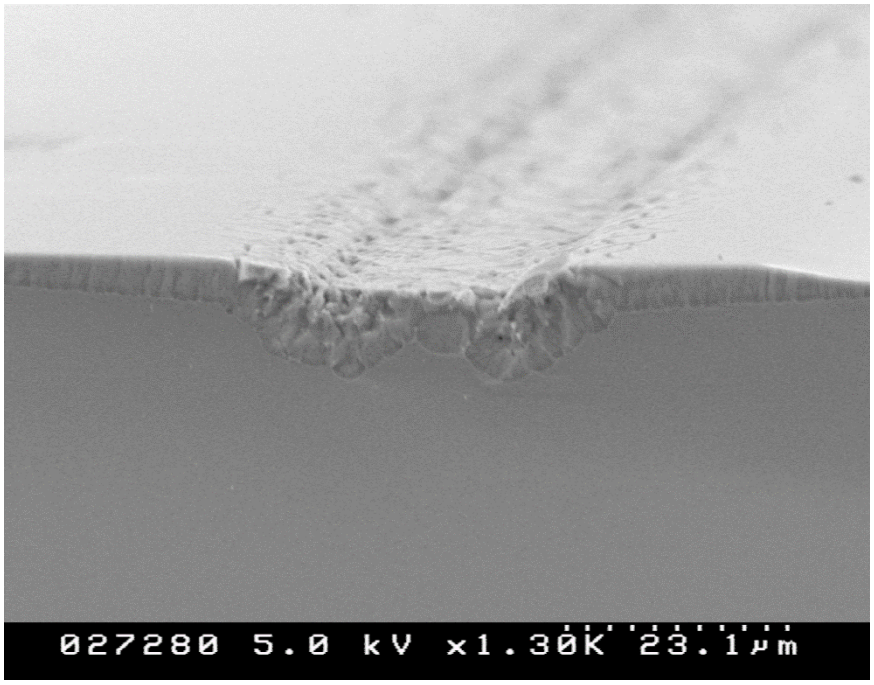

Fig. 6 SEM cross-sectional image showing the inhomogeneous PSi thickness that has been achieved using the sacrificial Pt approach

3.2 Anchored Pt Electrodes

In the standard metal-assisted aka galvanic etch we have used prior to this work, the Pt electrode is deposited on the Si wafer backside and a patterned Si_3N_4 layer is used as a mask to define the PSi areas on the front side of the wafer. With the anchored Pt electrode approach, the Si wafer backside is coated with Si_3N_4 to prevent etching on the back of the wafer. The front of the wafer still has a patterned Si_3N_4 layer exposing the Si that is to be converted to PSi. In addition, the front side also has openings for Pt deposited on top of the Si_3N_4 to make electrical contact to the Si wafer. As depicted in Fig. 7, patterned Pt electrodes are deposited on top of, and through holes in, the Si_3N_4 layer, so that the Pt electrodes have reliable adhesion throughout the PSi etch, and good electrical contact to the Si wafer.

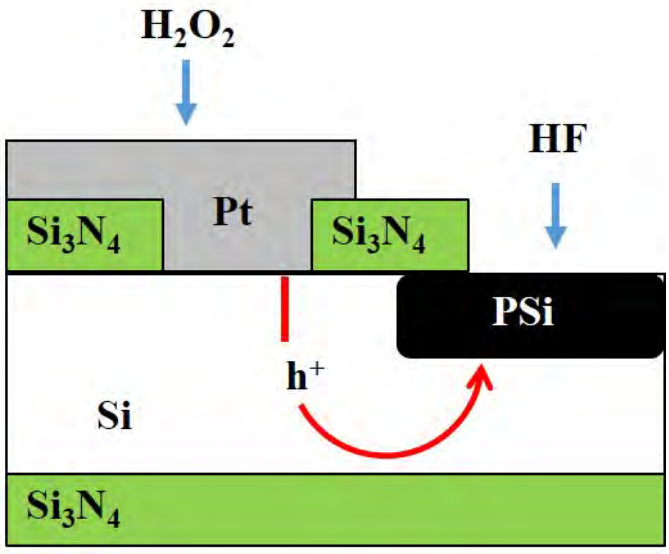

Fig. 7 Cross-sectional drawing of the anchored electrode structure and etch process depicting the PSi etch undercutting the Si_3N_4

The size and positions of the contact points to the Si are not critical except insofar as the proximity effect discussed below may cause variations in the PSi etch depth. The Si_3N_4 performs 2 important functions for this etch approach. As before, its resistance to the PSi etchant allows it to be used to define where the PSi will be etched. In addition, its dielectric nature prevents current crowding-increased etching or electropolishing at the edge of the Pt electrodes. As long as the Pt contact points are sufficiently far from the exposed Si, the etch current will spread out enough to reduce the likelihood of electropolishing at the near edge of the exposed Si.

As was seen with the sacrificial electrodes, electropolishing can occur if the H_2O_2 concentration is too high or if the Pt:Si ratio is too large. Figure 8 shows an example

of a line of etched PSi where the initial etching was near the electropolishing regime leading to broken and isolated pieces of PSi. As the etch progressed, the area of Si at the etch-front increased so that the etch current density decreased moving it farther from the electropolishing regime so that better quality PSi was formed.

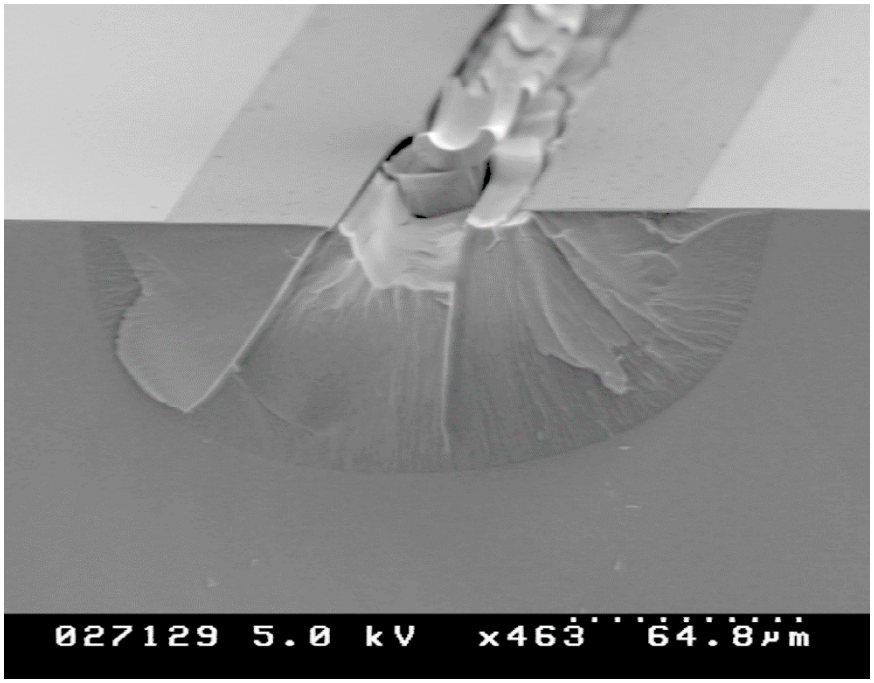

Fig. 8 SEM cross-sectional image showing signs of electropolishing early in the etch when there is a small area of Si being etched, while better PSi is formed as the etch-front reaches deeper in the Si when there is a larger area of Si being etched

There can also be transitions from higher etch rates to lower etch rates as a function of distance from the Pt electrode. This is essentially the same as the current crowding electropolishing seen at the edges of Pt electrodes with the sacrificial Pt etches. The only difference is that now, the Si_3N_4 mask layer determines where the Si is free to etch and depending on how far from the Pt electrode it is, there is a proportional additional resistance due to conduction through the wafer. This proximity effect can result in features closer to the Pt having different PSi etch rates and quality from features further from the Pt as can be seen in Fig. 9.

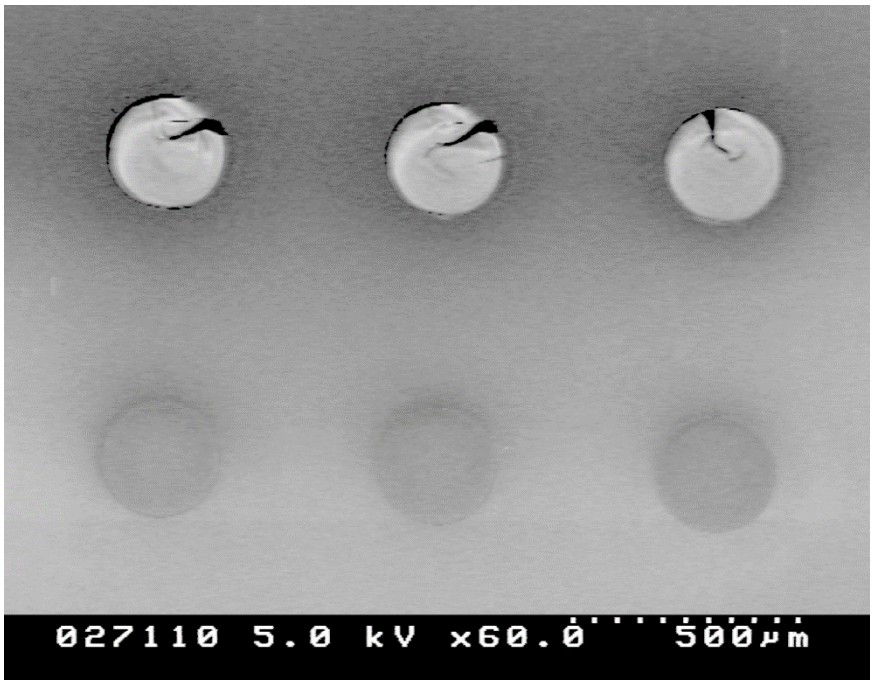

Fig. 9 SEM image showing cracked PSi circles formed closer to the Pt electrode (not shown, above the image) and more uniform PSi circles etched farther from the Pt electrode

A more quantitative measure of the proximity effect was made by etching a number of lines at various distances from a Pt electrode. Figure 10 shows a plot of line depth for 5 lines etched at different distances from Pt electrodes on 2 different samples. These line depths were measured using optical profilometry after the PSi was etch away with a KOH solution. It can be seen that there is a greater proximity effect when the PSi lines are etched close to the Pt electrode (Fig. 10a and b**)**. In this case, the etch depths ranging from 22.4 to 11.8 microns when the lines were from 2.1 to 3.9 mm from the nearest edge of the Pt contact point, respectively. In the second sample (Figs. 10c and d**)**, the etch depths vary from 7.3 to 6.5 microns for lines 20.1 to 21.9 mm from the Pt contact point, respectively. The additional resistance between the Pt electrode and the etched lines in this later sample results in more uniform etching as well as reduced etch rates.

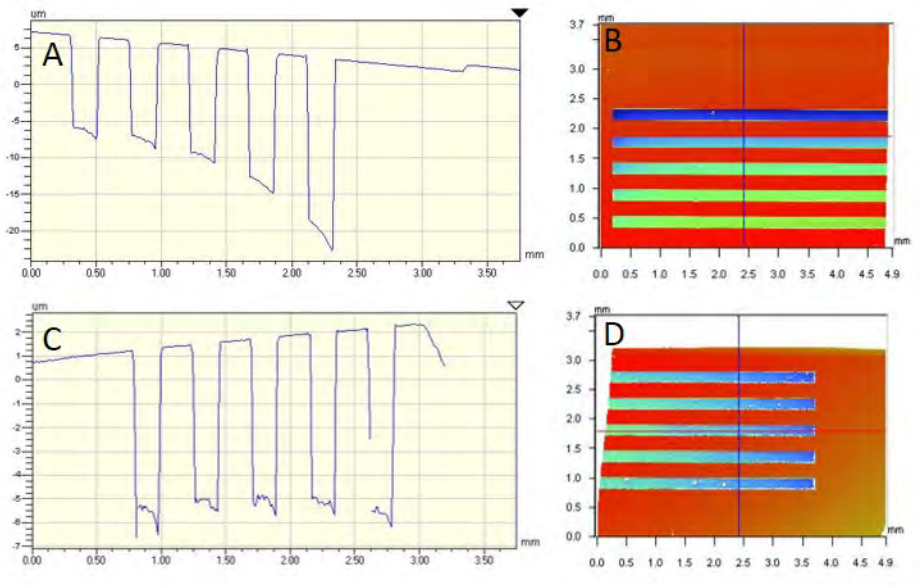

Fig. 10 Optical profilometry of PSi lines etched at various distances from the associated Pt electrode, which are to the right in the plots in A and C. A and B are the etch depths of 5 lines etched at 2.1, 2.55, 3.0, 3.45, and 3.9 mm from the nearest edge of the Pt electrode contact (not shown but above the image). C and D show lines etched at 20.1, 20.55, 21.0, 21.45, and 21.9 mm from the Pt electrode.

A simple voltage divider model serves as a first-order approximation for this effect, and it could be used to design electrodes for minimizing or utilizing differences in etch depth across the wafer. Taking the voltage divider model and scaling the output to match the largest etch depth in the experimental samples produces the results shown in Fig. 11. Figure 11 shows a significant difference between the model and experimental results at the further distances from the electrode. This disagreement may be simply due to sample to sample variation since there was some Pt electrode delamination from these samples; however, a more complicated model may also be required. For instance, there could be a systematic deviation due to differences in the etch depths. Such a result would be expected if the etch rate decreased with etch depth as might be expected due to increased resistance to etchant diffusion to the etch front as the PSi becomes thicker. However, an etch depth versus etch time measurement does not show a significant etch rate drop off with etch time over the etch depths used here. There are many other factors that need to be considered such as voltage drops, reaction kinetics, etc. More experimental measurements need to be made before a quantitative model can be developed.

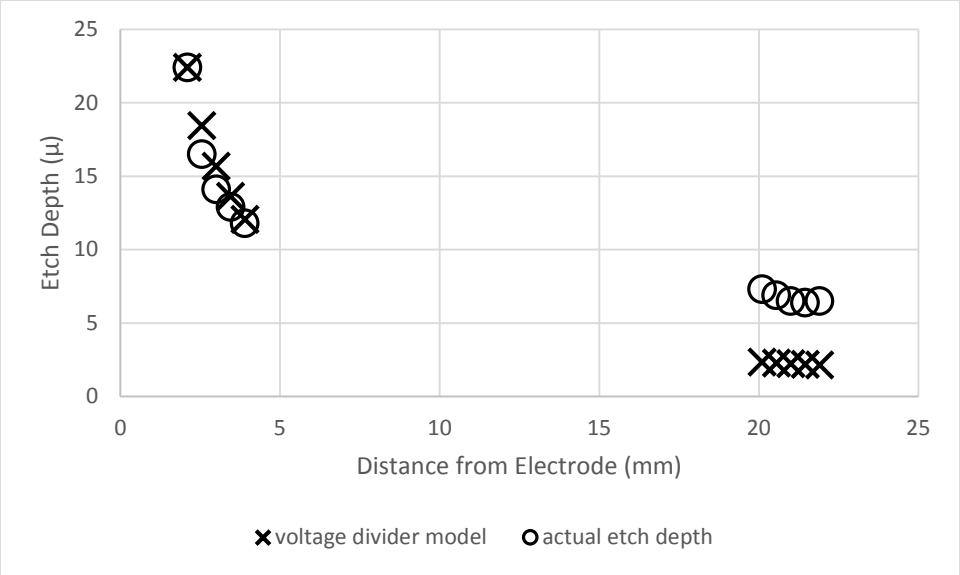

Fig. 11 Plot of etch depth vs. distance from the electrode data from Fig. 10 compared to predictions using a simple voltage divider model scaled to the deepest etch

Long straight line devices were made in order to characterize the burn properties of PSi produced with anchored Pt same-side electrodes. Using the high-speed camera to film the burning of a 0.5-mm-wide, 23-mm-long, and approximately 18-micron-thick PSi device, a flame speed of 3.6 m/s was measured using sodium perchlorate as the oxidizer. This is comparable to similar PSi etched using the standard backside electrode process, which produces m/s to km/s burn rates (Piekiel 2015).

Along with straight line PSi devices, serpentine devices with distances between lines down to 0.3 mm, including radii of curvatures down to 0.4 mm were etched. In these devices, the Pt electrical contact points were 0.25 mm away from the edge of the Si_3N_4 defining the PSi line, and the Pt:Si ratio was 1.5:1 in the straight sections. In the curved sections, the Pt:Si ratio varied between 0.688:1 and 3.94:1 depending on whether the associated Pt electrode was inside or outside of the PSi curve, respectively. Even with this large local variation in the Pt:Si ratio in the curves, there was no trend in PSi etch depth with local Pt:Si ratio observed. This is because the holes generated at the Pt surface easily conduct along the length of the Pt electrode so that there are no locally increased etch current densities. In order to vary the PSi etch rate along the serpentine, isolated Pt electrodes with different local Pt:Si ratios would have to be placed along the serpentine. Burning of serpentine devices was only partially successful. While burning proceeded around the curves, cross-talk between straight sections was observed so that areas further down the serpentine would ignite and then burn back towards the initial flame front as well as away from it. Eliminating this cross-talk is a difficult problem as it may be caused

by hot particles randomly falling back onto the sample, or by hot gases at the flame front jetting across to a nearby PSi line.

4. Conclusions

We have developed new procedures for etching PSi while potentially only exposing 1 side of the sample to the etch solution. This allows PSi devices to be more easily integrated with existing devices on the wafer or chip. These other devices may be used for initiating, controlling, or utilizing the output of the PSi devices. Of the 2 processes developed, the sacrificial electrode process is the simplest, not requiring a dielectric layer, but it produces an inhomogeneous PSi thickness across the wafer and introduces surface topography due to electropolishing that occurs at the electrode/etch-front interface. By adding a dielectric layer, which is resistant to the etch solution, more controllable etch depths and patterned devices are obtainable. One complication is that a proximity effect is observed where features closer to the electrode etch more rapidly. However, a simple voltage divider model can be used to predict the relative etch rates, and therefore, develop electrode patterns that will produce the desired results whether they include uniform or varied PSi etch depths. More work is required before a quantitative model for predicting etch depth will be possible. In order to vary the etch depth by varying the local electrode/Si ratio, the electrode will need to be cut up into electrically isolated sections or else the carriers will conduct along the length of the electrode causing more etching at the most easily reached exposed Si.

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List of Symbols, Abbreviations, and Acronyms

Ag	silver
Au	gold
Cu	copper
H_2O_2	hydrogen peroxide
HF	hydrofluoric acid
KOH	potassium hydroxide
Pd	palladium
PSi	porous silicon
Pt	platinum
SEM	scanning electron microscope
Si	silicon
Si_3N_4	silicon nitride
UV	ultraviolet

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